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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/773,847	02/05/2004	Dennis M. O'Connor	ITL1806US (P15392)	7172
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TROP, PRUNER & HU, P.C. 1616 S. VOSS RD., SITE 750 HOUSTON, TX 77057-2631			EXAMINER BATAILLE, PIERRE MICHEL	
			ART UNIT 2186	PAPER NUMBER
			MAIL DATE 06/26/2008	DELIVERY MODE PAPER

**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

# Office Action Summary

**Application No.**

10/773,847

**Applicant(s)**

O'CONNOR, DENNIS M.

**Examiner**

Pierre-Michel Bataille

**Art Unit**

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --  
**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 10 March 2008.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-24 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-24 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO/SF/ICE)  
Paper No(s)/Mail Date \_\_\_\_\_
- 4) ☐ Interview Summary (PTO-413)  
Paper No(s)/Mail Date \_\_\_\_\_
- 5) ☐ Notice of Informal Patent Application
- 6) ☐ Other: \_\_\_\_\_

## **DETAILED ACTION**

### ***Response to Amendment***

1. This Office Action is taken in response to Applicant's communication filed March 10, 2008 responding to Non-Final Rejection dated December 12, 2007. Applicant's amendments and/or arguments have been considered with the results that follow.
2. Claims 1-24 are pending the application under prosecution.

### ***Response to Arguments***

3. Applicant's arguments with respect to claims 1-24 have been considered but are not deemed to be persuasive for at least the following remarks.

The prior art noted below is made of record and not relied upon, but is considered pertinent to applicant's disclosure:

US 6,754,784 (North et al) teaching MMU including a translation look aside buffer (TLB), access control logic and translation-table-walking logic wherein: the primary functions of MMU 104 are the translation of virtual addresses into physical addresses and the control of accesses to memory; the TLB generally encaches 64 translated entries and provides the translation to the associated access control logic; Prefetch instruction is used to generate a modified virtual address upon a TLB miss with the descriptor generated from page table walk, using physical address bits from the accessed page table entry and index bits from the modified virtual address.

Claims 1-24 were rejected under 35 U.S.C. 102(b) as being anticipated by US 2002/0062434 (Chauvel) and applicant argues that in each processing device 14 has a unique requester identifier that is concatenated to a virtual address to form a modified virtual address. Applicant further argues that such modified virtual address is presented in every single case and that the modified address is used regardless of whether the virtual address-to-physical address translation for the virtual address does not exist in the storage.

Such assertion is simply not the case with considering Chauvel's disclosure. It is simply taught that translation misses in the TLB (translation lookaside buffer) and shared TLB trigger accesses to a translation table in external memory made using either a hardware mechanism or a software function. Chauvel teaches that an information corresponding to a current access, not contained in the TLB cache (i.e., a TLB-"miss" or "page fault"), must be retrieved from tables ("table walking"), located in main memory. "If there is a miss in the shared TLB 12, the virtual address is translated to a physical address through translation tables 16 (individually referenced as translation tables 16a-c in FIG. 1) in the physical memory 18." Chauvel teaches: each processing device having a unique requester identifier that is concatenated to a virtual address to form a modified virtual address with the concatenation performed in order to present unique virtual addresses to the shared TLB, the concatenated address provides a starting base address in the external memory's translation table.

Clauvel teaches, "The shared translation lookaside buffer generates a fault signal if a received virtual address is not related to an entry in the shared translation lookaside buffer. Responsive to a fault signal, translation logic determines physical address information based on the received virtual address ..."

In view of these remarks, the rejection is maintained and repeated below.

***Claim Rejections - 35 USC § 102***

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 1-24 are rejected under 35 U.S.C. 102(b) as being anticipated by US 2002/0062434 (Chauvel).

With respect to claim 1, Chauvel teaches the invention as claimed, memory management unit configured to receive a virtual address and provide a corresponding physical address **[(Known process or MMU (memory management unit) where several separate processing devices perform virtual address translation in order to access the physical memory) Par. 0007]**, the memory management unit comprising: an antenna **(general principle of hand held devices, i.e. inherent in all above noted appliances)**; a storage containing one or more virtual address-to-physical address translations **[TLB (translation lookaside buffer) provided as part of the MMU (memory management unit) caching recently accessed memory locations]**

**Par. 0007];** conversion logic to generate a modified virtual address from the virtual address if a virtual address-to-physical address translation for the virtual address does not exist in the storage **[(upon a TLB miss, unique requester identifier concatenated to a virtual address to form a modified virtual address, a starting base address in the external memory translation table] Par. 0008 & 0007];** and a page table walk unit configured to convert the modified virtual address into the corresponding physical address **[(when a TLB (translation lookaside buffer) cache does not contain the information corresponding to the current access (i.e., a TLB-"miss" or "page fault"), the information must be retrieved from tables ("table walking"), located in main memory) Par. 0007].**

With respect to claims 2-3, Chauvel teaches the invention as claimed, the memory management unit wherein the conversion logic is configured to replace one or more bits of the virtual address with a process identifier if the one or more bits comprises a predetermined value **[(virtual address records and corresponding descriptor records include a resource identifier (R\_ID) field, a task identifier (Task\_ID) field, used to invalidate entry associated with specific tasks, the task identifier identifies all entries in a TLB belonging to a specific task) Par. 0032 & 0031].**

With respect to claim 4, Chauvel teaches the invention as claimed, the memory management unit wherein the memory management unit is configured to receive the

virtual address from an arithmetic logic unit **[(digital signal processor, multiprocessor logic capable of computing) Par. 0024-0026].**

With respect to claim 5, Chauvel teaches the invention as claimed, the memory management unit wherein the memory management unit is configured to receive the virtual address from an incrementor **[(digital signal processor, multiprocessor logic capable of computing) Par. 0024-0026].**

With respect to claim 6, Chauvel teaches the invention as claimed, the memory management unit wherein the virtual address comprises a data address **[(virtual address records and corresponding descriptor records include a resource identifier (R\_ID) field, a task identifier (Task\_ID) field, used to invalidate entry associated with specific tasks, the task identifier identifies all entries in a TLB belonging to a specific task) Par. 0032 & 0031].**

With respect to claim 7, Chauvel teaches the invention as claimed, the memory management unit wherein the virtual address comprises an instruction address **[(virtual address records and corresponding descriptor records include a resource identifier (R\_ID) field, a task identifier (Task\_ID) field, used to invalidate entry associated with specific tasks, the task identifier identifies all entries in a TLB belonging to a specific task) Par. 0032 & 0031].**

With respect to claim 8, Chauvel teaches the invention as claimed, the memory management unit wherein the one or more virtual address-to-physical address translations are invalidated upon updates to a process identifier **[(virtual address**

**records and corresponding descriptor records include a resource identifier (R\_ID) field, a task identifier (Task\_ID) field, used to invalidate entry associated with specific tasks, the task identifier identifies all entries in a TLB belonging to a specific task) Par. 0032 & 0031].**

With respect to claim 10, Chauvel teaches the invention as claimed, the memory management unit wherein the storage is configured to store one or more most recently generated virtual address-to-physical address translations [(virtual address records and corresponding descriptor records include a resource identifier (R\_ID) field, a task identifier (Task\_ID) field, used to invalidate entry associated with specific tasks, the task identifier identifies all entries in a TLB belonging to a specific task) Par. 0032 & 0031].

With respect to claims 11-24, the claims correspond in scope to claims 1-10; therefore, the claims are rejected under the same assumption.

### ***Conclusion***

6. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any



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extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Pierre-Michel Bataille whose telephone number is (571) 272-4178. The examiner can normally be reached on Mon, Tue-Fri (8:00A to 5:30P).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew M. Kim can be reached on (571) 272-4182. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Pierre-Michel Bataille/  
Pierre-Michel Bataille  
Primary Examiner  
Art Unit 2186

